Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT –**
2. **INPUT +**
3. **V –**
4. **OUTPUT**
5. **V +**

**.071”**

**.054”**

**1**

**2**

**3**

**5**

**4**

**LMC6082**

**C**

**DIE ID**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V + (may also be left FLOATING)**

**Mask Ref: LMC6082 C**

**APPROVED BY: DK DIE SIZE .054” X .071” DATE: 7/7/22**

**MFG: NATIONAL THICKNESS .013” P/N: LMC6081C**

**DG 10.1.2**

#### Rev B, 7/19/02